TRIGGER BOARD

FIBER TRANSCIEVERS
AFBR-57R5AEZ
TLK3101

CLOCK DISTRIBUTION

KOTO CONTROLS

FLIP-FLOP

XILINX MAIN BLOCKS

JTAG PORT

DOR2 MEMORY

ETHERNET PORT

ETHERNET PHY

XILINX SLAVE BLOCKS

LOCAL OSC.

XILINX CONFIGURATION

DIAGNOSTICS

POWER SUPPLIES

VME INTERFACE

XILINX SLAVE BLOCKS

SUM IN BUS

SUM OUT BUS

ETHERNET PHY

ETHERNET PORT

POWER SUPPLIES

KOTO CONTROLS

FLIP-FLOP

XILINX MAIN BLOCKS

DIAGNOSTICS

VME INTERFACE

XILINX MAIN BLOCKS

TITLE: TRIGGER BOARD
FILENANE: TRIGGER-REV-C2.sch
REVISION: C2
DRAFTED: 12/1/2010
DATING: 12/01/2010
CHECKED: KOTO
QUALITY CONTROL: <QC By>
RELEASD: <Released By>
DRAWING NO: 0001
COMPANY: Univ. of Michigan - Physics
SHEET: 1 OF 40
KOTO_PTP#: Point-to-point
from daisy-chain slots to slot 12
KOTO_BUS#: Bused signals
from daisy-chain slots to slot 12

L2CAL Backplane P3 (P5+P6) connector
Daisy-chain slots: 4,5,6 - 9,10,11 - 13,14,15 - 19, 18, 20
Start at slot 4 and 20 and end up in slot 12

Corrected text re: backplane routing

GND
SUM_IN[0:23]
SAVED:
REV:
DRAWN:
DATED:
CHECKED:
QUALITY CONTROL:
RELEASED:
COMPANY:
FILE:
REVISION RECORD:
ECO:
ECO NO:
REVISION RECORD:
APPROVED:
DATE:

ECO: C1-001
Corrected text re: backplane routing
VME (TTL) to Xilinx I/O

VME Address

VME Control

VME Data

Title: TRIGGER BOARD
Drawing: J.Ameei
Checked: KOTO
Quality Control: <QC By>
Released: Released By
Drawing No: 0001
Scale: 1:1
Size: B

FILENAME: TRIGGER-REV-C2.sch
Saved: 12/1/2010
Dated: 10/8/2010
12/1/2010
12/1/2010
<QC Date>
<Release Date>
<Company: Univ. of Michigan - Physics>
Sheet: 6 OF 40
JTAG CHAIN OVERVIEW

P7 JUMPER ALLOWS FPGA2 TO BE BYPASSED

JTAG HEADER

32MB FLASH PROM

PROM TEST POINTS

VCCO Decoupling Not Needed for FX70T package. (see UG203 p.15)
External Decoupling for FX70T package (see UG203 p.15)
External 125 MHz (8 ns) Oscillator

U66 Jumper Settings

Global Clock Banks

**External 125 MHz (8 ns) Oscillator**

- **Title:** External 125 MHz (8 ns) Oscillator
- **Company:** K0TO

**U66 Jumper Settings**

- **Jumper Settings:**
  - JP17: OFF
  - JP18: ON

**Global Clock Banks**

- **Bank 3**
  - **XC5VFX70T-FFG1136**
  - **XC5VFX70T-FFG1136C**

- **Bank 4**
  - **XC5VFX70T-FFG1136**
  - **XC5VFX70T-FFG1136C**

**Note:**
- **Additional Information:**
  - **XC5VFX70T-FFG1136** or **XC5VFX70T-FFG1136C**
  - **Component Details:**
    - **Number of Pins:** 28
    - **pinout:**
      - **I/O Pins:**
        - **VCCO_3_1**
        - **VCCO_3_2**
        - **VCCO_4_1**
        - **VCCO_4_2**
      - **Ground:**
        - **GND**
    - **Package:** FPGA

**Legend:**
- **Component Markings:**
  - **5-pin Header P8:**
    - **Description:**
      - **Function:**
        - **CLK125-FPGA-IN**
      - **Additional Details:**
        - **Description:**
          - **SOP65P640X110-16N**

**ECO Notes:**
- **ECO No.:**
  - **C1-005**
  - **C1-006**
  - **C1-007**

**Revision:**
- **Date:**
  - **10/8/2010**
  - **12/01/2010**

**Technical Details:**
- **Clock Source:**
  - **CLK125-BKPLN**
  - **Additional Notes:**
    - **Description:**
      - **Local 125 Osc. independent of U66 (CLK125-OSC)**
      - **Added Clock Mux U66 to choose FPGA source clock (CLK125-FPGA-IN)**
      - **Replace spare testpoints with 5 pin header P8, added more spare ports**

**Qualification:**
- **Approval:**
  - **<QC By>**
  - **<Released By>**

**Company:**
- **Univ. of Michigan - Physics**

**Sheet:**
- **15 of 40**
125MHz directly from FPGA - Signal 0

Clocks to TLK3101

125MHz directly from FPGA - Signal 1
One decoupling cap each VCC pin.
One decoupling cap each VCC pin.
One decoupling cap each VCC pin.
One decoupling cap each VCC pin.
One decoupling cap each VCC pin.
One decoupling cap each VCC pin.
FPGA must drive GMII_GBE_RST high for U30 to leave reset state.

Place R275...288 close to PHY

Biases

Two power supplies needed: 1.8V for core and 2.5V(3.3V) for IO
Device Configuration Settings

TIA/EIA 568B wiring is done internally
MD(x)+/- are connections to magnetics, not RJ45 pins

Magnetics and RJ45

LEDs for linking ethernet connection

CONFIGURATION JUMPERS / LED INDICATORS

ECO:     C1-017
CHANGED LED CUTTENT LIMITING FROM 330 TO 390

ECO:     C1-008
CHANGED LED CUTTENT LIMITING FROM 330 TO 390

ERJ-3EKF3900V
RESC1608X38N
LEDC1608X80N

LTST-C190KGKT
Lite-On

1%
INPUT FUSES, LEDS, TESTPOINTS

TRANSIENT VOLTAGE SUPPRESSION

+5V to 2.5, 1.2, 1.0V @ 6 A Max and LEDs
+3.3V to 1.8V @ 6 A Max and LEDs

Connect ADJ between pin 5 and pin 1 using dedicated traces. Fix ADJ as close as possible to pin 5. Do not connect CAP from pin 5 to either GND or pin 6.

PM5 LAYOUT NOTES

CTN-LEDs placed close to each other, pin 2 as positive. CV2s placed close to each other, pin 3 as possible. Pin 5 connected to COUT, separate trace from COUT. COUT negative leads tied to GND, then to GND.

C351/C352/C353/C349/C347/C346/C350:
Pos. terminal connect directly to pin, do not use a VIA. Neg. terminal connect directly to GND, do not use a VIA. Neg. node of C346/C347/C349 and C351 should be tied together.

DRAWN: I.Ameel
DATING: 06/2010
DIAGNOSTIC HEADER
AMP 5-5179009-6

Geo Address: 5 MSB address bits
REPLACED 1 kΩ AMP 5-179009-6 WITH CONNECTORLESS PROBE PORTS X4

CONNECTORLESS DIAGNOSTIC PORTS

CONNECTORLESS TEST FIXTURE
2.5V VCCO Decoupling Bank 8

External 200 MHz (5 ns) Oscillator

2.5V 200MHz DECOUPLING

Place termination close to FPGA
Place R264..R274 close to FPGA.
Termination as specified in Xilinx UG079 p.51 for DDR2 memory

- Added biasing resistors to all signals based on Xilinx Memory Interface Generator.
- Capacitors:
  - C2: 0.01 μF
  - C3: 0.001 μF
  - C4: 0.001 μF
  - C5: 0.001 μF
  - C6: 0.001 μF
  - C7: 0.001 μF
  - C8: 0.1 μF
  - C9: 0.001 μF
  - C10: 0.001 μF
  - C11: 0.001 μF
  - C12: 0.001 μF
  - C13: 0.001 μF
  - C14: 0.001 μF

- Resistors:
  - R256 to R263: 49.9 kΩ, 1% tolerance
  - R337: 49.9 kΩ, 1% tolerance
  - R338: 49.9 kΩ
  - R339: 49.9 kΩ
  - R340: 49.9 kΩ
  - R341: 49.9 kΩ
  - R342: 49.9 kΩ
  - R343: 49.9 kΩ
  - R344: 49.9 kΩ
  - R345: 49.9 kΩ
  - R346: 49.9 kΩ
  - R347: 49.9 kΩ
  - R348: 49.9 kΩ
  - R349: 49.9 kΩ
  - R350: 49.9 kΩ
  - R351: 49.9 kΩ
  - R352: 49.9 kΩ
  - R353: 49.9 kΩ
  - R354: 49.9 kΩ
  - R355: 49.9 kΩ
  - R356: 49.9 kΩ
  - R357: 49.9 kΩ
  - R358: 49.9 kΩ
  - R360: 49.9 kΩ
  - R361: 47 kΩ, 1% tolerance

- Voltage references:
  - VCC1V8
  - VREF_0V9
  - GND

- DDR2 Memory - 0
Termination as specified in Xilinx UG079 p.51 for DDR2 memory