L2CAL Backplane P3 (P5+P6) connector

Daisy-chain slots: 3,4,5 - 8,9,10 - 12,13,14 - 17,18,19
Start at slot 3 and 19 and end up in slot 11

daisy-chained input signals

daisy-chained output signals
NOTE:
K0TO_DONE IS AN OPEN-COLLECTOR SIGNAL (NOMINALLY PULLED UP)
IT FUNCTIONS AS A LOGICAL 'AND' FOR K0TO DONE STATUS.
ANY BOARDS ASSERTING K0TO_DONE RENDER THE SYSTEM NOT DONE.
MOST P2 BACKPLANE SIGNALS ARE OPEN COLLECTOR.
THEY ARE INDICATED AS ACTIVE LOW DUE TO NOMINAL PULLUP FOR OPEN COLLECTOR.
THEIR ASSIGNMENT AND FUNCTION IS DETERMINED WITHIN THE MASTER CONTROL
BOARD AND RECEIVED BY THE LOCAL FPGA.
External Decoupling for FX70T package (see UG203 p.15)

VCC AUX

VCCINT

33uF

CAPMP3528X210N

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One decoupling cap each VCC pin.
GPB Transceiver 2

- Channels 2, 3
- Texas Instrument QFP50P1200X1200X100-65N
- One decoupling cap each VCC pin.

GPB Transceiver 3

- Channels 2, 3
- Texas Instrument TLU3101IRCP QFP50P1200X1200X100-65N
- One decoupling cap each VCC pin.
One decoupling cap each VCC pin.
One decoupling cap each VCC pin.
One decoupling cap each VCC pin.
25 MHz Crystal

Biases

Two power supplies needed: 1.8V for core and 2.5V(3.3V) for IO

NOTE: FPGA must drive GMII_GBE_RST high for U30 to leave reset state
Device Configuration Settings

Magneatics and RJ45

LEDs for linking ethernet connection

CONFIGURATION JUMPERS / LED INDICATORS
INPUT FUSES, LEDS, TESTPOINTS

TRANSIENT VOLTAGE SUPPRESSION

+5V to 2.5, 1.2, 1.0V @ 6 A Max and LEDs

+3.3V to 0.9V @ 3 A Max and LEDs

Connect ADI between pin 5 and pin 1 using dedicated traces.
Place ADI as close as possible to pin 5.
Do not connect CAP from pin 5 to either GND or pin 6.

PM5 LAYOUT NOTES

C351/C352/C353/C349/C347/C346/C350:
Pos. terminal connect directly to pin, do not use a VIA
Neg. terminal connect directly to DGND, do not use a VIA
Neg. node of C346/C347/C349 and C351 should be tied together

-5V UNFUSED

VOSNS

REFIN

TI_TPS51200DRC

REV:

SHEET:

FILENAME:
TRIGGER-REV-B4.sch

TITLE:
TRIGGER BOARD

QUALITY CONTROL:
KITO

DATE:
06/10/2010

SHEET:
30 OF 39

COMPANY:
Univ. of Michigan - Physics

D  E  F  G  H

A

B

C

D

E

F

G

H

DATE:
06/17/2010

APPROVED:
06/2010

APPROVED:
06/17/2010

ECO NO:

REVISION RECORD

ECO:

REV:

DRAWING NO:

<Released By>

<Drawing Number>

ECO:

REV:

DRAWING NO:

<Released By>

<Drawing Number>

ECO:

REV:

DRAWING NO:

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<Released By>

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CONNECTORLESS DIAGNOSTIC PORTS

DRAWN: M. Tecchio
DATED: 06/10/2010

REPLACED 140p AMP 5-179009-6 WITH CONNECTORLESS PROBE PORTS X4

ECO: 83-011
CONNECTORLESS TEST FIXTURE
1.8V VCCO Decoupling Bank 6

1.8V VCCO Decoupling Bank 3
VIRTEX TO VIRTEX DATA EXCHANGE

Place termination close to FPGA

SLAVE FPGA CLOCKS

2.5V VCCO Decoupling Bank 3

External 200 MHz (5 ns) Oscillator

2.5V VCCO Decoupling Bank 8

2.5V 200MHz DECOUPLING