NOTE:
KOTO STATUS Signals injected on to P2 backplane by local buffers on sheet 32. These signals are inverted logic.
L2CAL Backplane P3 (P5+P6) connector

Daisy-chain slots: 4,5,6 - 9,10,11 - 13,14,15 - 18,19,20
Start at slot 4 and 20 and end up in slot 12

KOTO_BUS# : Bused signals
KOTO_PTP# : Point-to-point

SUM_LEFT[0:23]  SAVED:

SUM_RIGHT[0:23]  DRAWN:

GND
text
External Decoupling for FX30T package (see UG203 p.15)
External 125 MHz (8 ns) Oscillator

Global Clock Banks
FPGA must drive GMII_GBE_RST high for U30 to leave reset state.
Device Configuration Settings

Magneetics and RJ45

LEDs for linking ethernet connection

CONFIGURATION JUMPERS / LED INDICATORS
INPUT FUSES, LEDS, TESTPOINTS

TRANSIENT VOLTAGE SUPPRESSION

+5V to 2.5, 1.0V @ 6 A Max and LEDs
+3.3V to 1.8V @ 6 A Max and LEDs

Connect ADJ between pin 5 and pin 1 using dedicated traces.
Place ADJ as close as possible to pin 5.
Do not connect CAP from pin 5 to either GND or pin 6.

+5V to 2.5, 1.0V @ 6 A Max and LEDs
+3.3V to 1.8V @ 6 A Max and LEDs
Copper Discharge Strips

Front Panel Reset

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Copper Discharge Strips

Front Panel Reset

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Front Panel Reset

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Front Panel Reset

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Copper Discharge Strips

Front Panel Reset

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Copper Discharge Strips

Front Panel Reset

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NOTE:
KOTO STATUS REGISTER SIGNALS ARE POSITIVE LOGIC WHENGENERATED BY MASTER BOARD. THEY MUST BE INVERTED LOGIC ON THE P2 BACKPLANE.
CROSS CONNECTING +/- SIGNALS WITH +/- PORTS GIVES AND INVERTED LOGIC OUTPUT FROM LVDS RECEIVERS.

NOTE:
125MHz CLOCK AND L1A ARE RECEIVED AS LVDS BUT TRANSMITTED ON THE BACKPLANE AS LVPECL. PCB CONVERTS LVDS TO LVTTL NEAR THE FRONT PANEL. CONVERTS LVTTL TO LVPECL CLOSER TO THE BACKPLANE.
LVTTL TO TTL BACKPLANE DRIVER

LVTTL TO LVPECL DRIVER
Remove U88 and U59 to disable MACTRIS from driving L1A and CLK125 on the VME backplane

LVTTL TO TTL DRIVER ENABLE
Remove JP16 to disable MACTRIS from driving 27 CHIE signals on the VME backplane
FRONT PANEL LEMO
NIM level signals
Active = 0.8V
Inactive = 0V

NIM DECODING THRESHOLD
Adjust R88 to set threshold

THRESHOLD COMPARISON
Circuit is a modification on LM311 Datasheet
"Zero Crossing Detector Driving MOS Logic"

CMOS OUTPUT
Bias/Pullup/Pulldown as needed